trench-periphery portion **132**B recedes from the edge of the trench **102***a*. Therefore, as shown in FIG. **13**, the inclination θ**3** of the top end portion of the trench **102***a* in contact with the end of the trench-periphery portion **132**B is smaller than the inclination θ**1** of the inclined portion of the trench-periphery portion **132**B before formation of the first insulating film **131**. FIG. **13** is an enlarged cross-sectional view of a third alteration of the semiconductor device of the embodiment. In this case, the virtual aspect ratio of the trench **102***a* at the time of embedding of the conductive film **105**A becomes small, and this further facilitates embedding of the conductive film **105**A.

[0086] In this embodiment, described was the example of forming the first insulating film **131** after formation of the second insulating film **132**. The formation of the first insulating film **131** after formation of the second insulating film **132** provides an advantage that the first insulating film **131** is free from degradation in film quality that may otherwise occur if the first insulating film **131** is exposed to high-density plasma. This also provides an advantage that the thickness of the first insulating film **131** will not be reduced by high-density plasma. However, the first insulating film **131** may be formed first before formation of the second insulating film **132**. FIGS. **14** to **16** are cross-sectional views showing a fourth alteration of the fabrication process for a semiconductor device of the embodiment. An SiO_2 film formed by the HDP-CVD method is more likely to cause generation of fixed charge, etc. at the interface with the semiconductor layer than an SiO_2 film formed by the thermal oxidation method. By forming the first insulating film **131** by the thermal oxidation method prior to formation of the second insulating film **132**, it is possible to obtain an advantage that generation of fixed charge at the interface between the gate insulating film **103** and the semiconductor layer **102** can be prevented or reduced.

[0087] In this alteration, as shown in FIG. **14**, after formation of the trench **102***a*, thermal oxidation is performed before formation of the second insulating film **132**, to form the first insulating film **131** on the exposed portion of the semiconductor layer **102**. Thereafter, as shown in FIG. **15**, the second insulating film **132** is formed on the bottom of the trench **102***a* and the periphery thereof by the HDP-CVD method. Then, as in the case of forming the second insulating film **132** before the first insulating film **131**, formation of the gate electrode **105**, formation of the source electrode **106**, formation of the drain electrode **107**, etc. may be performed.

[0088] In the case of forming the first insulating film **131** before the second insulating film **132**, as shown in FIG. **16**, the position of the end of the trench-periphery portion **132**B of the second insulating film **132** corresponds with the top edge of the trench **102***a* after formation of the first insulating film **131**. In other words, the position of the end of the trench-periphery portion **132**B and the position of the portion of the first insulating film **131** corresponding to the top edge of the trench **102***a* correspond with each other. The formation of the first insulating film **131** before the second insulating film **132** can also be applied even when the top end portion of the trench **102***a* is rounded. FIG. **17** is a cross-sectional view showing a fifth alteration of the semiconductor device of the embodiment. In this case, as shown in FIG. **17**, the inclination θ**4** of a portion of the trench **102***a* having the first insulating film **131** formed thereon that is in contact with the end of the trench-periphery portion **132**B corresponds with the inclination θ**1** of the inclined portion of the trench-periphery portion **132**B.

[0089] In the case of forming the first insulating film **131** before the second insulating film **132**, also, wet etching may be performed after formation of the second insulating film **132**. By performing wet etching, it is ensured to expose the first insulating film **131** on the side of the trench **102***a*, to bring the first insulating film **131** into contact with the gate electrode **105** on the side of the trench **102***a*. FIG. **18** is a cross-sectional view showing a sixth alteration of the semiconductor device of the embodiment. When the second insulating film **132** is wet-etched, as shown in FIG. **18**, the end of the trench-periphery portion **132**B recedes from the top edge of the trench **102***a* after formation of the first insulating film **131** by t**4**. The receding amount t**4** of the trench-periphery portion **132**B approximately corresponds with the etching amount of the second insulating film **132**. Thirty percent or less of the thickness of the second insulating film **132** will be enough as the etching amount of the second insulating film **132**. In addition, in this case, since the first insulating film **131** has been formed also on the periphery of the trench **102***a*, there will be little influence on the gate capacitance as far as the receding amount t**4** is about 100 nm or less.

[0090] Moreover, as shown in FIG. **19**, wet etching of the second insulating film **132** may be performed even when the top end portion of the trench **102***a* is rounded. FIG. **19** is a cross-sectional view showing a seventh alteration of the semiconductor device of the embodiment. In this case, the inclination θ**5** of a portion of the trench **102***a* having the first insulating film **131** formed thereon that is in contact with the end of the trench-periphery portion **132**B is smaller than the inclination θ**1** of the inclined portion of the trench-periphery portion **132**B.

[0091] The thickness of the first insulating film **131** changes with the plane direction of the semiconductor layer **102**. When the semiconductor layer **102** is formed on the substrate **101** having the (0001) Si plane as the principal surface, the thickness of the portions of the first insulating film **131** formed on the top surface of the semiconductor layer **102** and the bottom of the trench **102***a* is smaller than the thickness of the portion thereof formed on the side of the trench **102***a*. However, the thin first insulating film **131** will cause no problem because the second insulating film **132** is to be formed on the bottom of the trench **102***a* and the periphery thereof.

[0092] While the n-type MISFET was described in this embodiment, a p-type MISFET can also be formed. In this case, the conductivity type of the substrate **101**, the drift region **121**, and the source region **124** may be changed to the p-type and that of the body region **123** to the n-type. Also, the semiconductor layer **102** may have a region other than the drift region **121**, the body region **123**, and the source region **124**. For example, for reducing the electric field, an impurity layer having a conductivity type different from the drift region **121** may be provided near the bottom of the trench **102***a*.

[0093] While the MISFET having an inverted channel structure was described in this embodiment, a similar configuration can also be used for a MISFET having a stored channel structure as shown in FIG. **20**. FIG. **20** is a cross-sectional view showing an eighth alteration of the semiconductor device of the embodiment. For example, after formation of the trench **102***a* in the semiconductor layer **102**, a channel layer **125** made of an n-type SiC layer may be formed on the semiconductor layer **102** including the inside of the trench **102***a*. After formation of the channel layer **125**, the